<u>Amendments to the Claims</u>:

This listing of claims will replace all prior versions, and listings, of claims in the application:

<u>Listing of Claims</u>:

Claim 1 (original) A MAP decoder, comprising:

(a) inputs for receiving symbols;

(b) a forward recursion block coupled to said inputs, said forward recursion block with cascade architecture;

(c) a backward recursion block coupled to said inputs; said backward recursion block with cascade architecture; and

(d) an output block coupled to said forward recursion block and to said backward recursion block.

Claim 2 (currently amended) The decoder of claim 1, wherein:

(a) said forward recursion block includes first parallel add-compare-<u>select</u> ~~elect~~ (ACS) units, second parallel ACS units, and a first transformation unit connecting the outputs of said first ACS units to inputs of said second ACS units;

(b) said backward recursion block includes third parallel ACS units, fourth parallel ACS units, and a second transformation unit connecting the outputs of said first ACS units to inputs of said second ACS units; and

(c) said output block couples to the inputs of said ACS units and to said inputs for receiving symbols.

Claim 3 (original) The decoder of claim 1, further comprising:

(a) an input for extrinsic information coupled to said forward recursion and backward recursion blocks.

Claim 4 (original) A MAP decoder, comprising:

(a) inputs for receiving symbols from an encoder with 2^{n+m} states where n and m are positive integers;

(b) a forward recursion block coupled to said inputs, said forward recursion block with m+1 first sets of add-compare-select (ACS) units, each of said first sets including 2^n ACS units in parallel, said m+1 first sets coupled in series with feedback;

(c) a backward recursion block coupled to said inputs, said backward recursion block with m+1 second sets of ACS units, each of said second sets including 2^n ACS units in parallel, said m+1 second sets coupled in series with feedback; and

(d) an output block coupled to said first sets and said second sets of ACS units.

Claim 5 (original) The decoder of claim 4, wherein:

(a) each of said ACS units includes 1 2-input max* block; and

(b) said output block includes $2(m+1)2^n$ 2-input max* blocks.

Claim 6 (original) A turbo decoder, comprising,

(a) a first MAP decoder with inputs for receiving symbols and extrinsic information;

(b) a first interleaver coupled to an output of said first MAP decoder;

(c) a second interleaver coupled to said inputs for receiving symbols;

(d) a second MAP decoder with inputs coupled to outputs of said first and said second interleavers and to said inputs for receiving symbols;

(e) a deinterleaver coupled to an output of said second MAP decoder; and

(f) a decision unit coupled to said inputs for receiving symbols and outputs of said first MAP decoder and of said deinterleaver;

(g) wherein said first and said second MAP decoders each includes

(i) a forward recursion block, said forward recursion block with cascade architecture;

(ii) a backward recursion block, said backward recursion block with cascade architecture, and (iii) an output block coupled to said forward recursion block and to said backward recursion block.

Claim 7 (original) The decoder of claim 6, wherein:

(a) the output of said deinterleaver couples to said input for extrinsic information of said first MAP decoder to provide feedback for iterative operation.